AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An image sensor readout circuit, comprising:

a column line for receiving a plurality of analog pixel and analog reset signals; and

a binning circuit coupled to said column line, wherein said binning circuit comprises:

a first plurality of charge storage devices for respectively storing a predetermined plurality of analog pixel signals from a plurality of pixels,

a first combining circuit for combining said stored ~~combines a predetermined~~ plurality of analog pixel signals ~~from a plurality of pixels~~ and ~~outputs~~ outputting them on a first output line, [[and]]

a second plurality of charge storage devices for respectively storing a predetermined plurality of analog reset signals from a plurality of pixels, and

a second combining circuit for combining said stored ~~combines a predetermined~~ plurality of analog reset signals ~~from a plurality of pixels~~ and ~~outputs~~ outputting them on a second output line.

2. (Canceled)

3. (Currently Amended) The readout circuit of claim 2, wherein ~~said first sample circuit comprises~~:

said first combining circuit comprises a first plurality of sample switches; and

said first plurality of charge storage devices comprises a first plurality of capacitive elements, and

~~wherein~~ each of said first plurality of sample switches [[are]] is coupled to a respective one of said first plurality of capacitive elements, said first plurality of capacitive elements being further coupled to the first output line.

4. (Currently Amended) The readout circuit of claim 3, wherein ~~said second sample circuit comprises~~:

said second combining circuit comprises a second plurality of sample switches[[; and]],

wherein said second plurality of charge storage devices comprises a second plurality of capacitive elements, and

~~wherein~~ each of said second plurality of sample switches [[are]] is coupled to a respective one of said second plurality of capacitive elements, said second plurality of capacitive elements being further coupled to the second output line.

5. (Previously Presented) The readout circuit of claim 4, wherein said first and second plurality of sample switches and capacitive elements comprise an even number of sample switches and capacitive elements.

6. (Currently Amended) A binning circuit for an image sensor, comprising:

a column line for receiving analog pixel and analog reset signals of an active pixel sensor;

a first sample circuit coupled to said column line, said first sample circuit comprising a first plurality of charge storage devices respectively storing a plurality of analog pixel signals from a plurality of pixels;

a second sample circuit coupled to said column line, said second sample circuit comprising a second plurality of charge storage devices respectively storing a plurality of analog reset signals from a plurality of pixels;

a first switch coupled to said first sample circuit and to a first output line, said first switch being controlled to combine said stored plurality of analog pixel signals and output said combined pixel signals on said first output line; and

a second switch, coupled to said second sample circuit and to a second output line, said second switch being controlled to combine said stored plurality of analog reset signals and output said combined reset signal on said second output line.

7. (Currently Amended) The binning circuit of claim 6, wherein said first sample circuit further comprises:

a first plurality of sample switches[[; and]],

wherein said first plurality of charge storage devices comprises a first plurality of capacitive elements, and

wherein each of said first plurality of sample switches [[are]] is coupled to a respective one of said first plurality of capacitive elements, said first plurality of capacitive elements being further coupled to the first output line.

8. (Currently Amended) The binning circuit of claim 7, wherein said second sample circuit further comprises:

a second plurality of sample switches[[; and]],

wherein said second plurality of charge storage devices comprises a second plurality of capacitive elements, and

wherein each of said second plurality of sample switches [[are]] is coupled to a respective one of said second plurality of capacitive elements, said second plurality of capacitive elements being further coupled to the second output line.

9. (Previously Presented) The binning circuit of claim 8, wherein said first and second plurality of sample switches and capacitive elements comprise an even number of sample switches and capacitive elements.

10. (Currently Amended) A method of binning an output of an active image sensor, comprising:

sampling and respectively storing analog output signals from a plurality of pixels of said sensor according to a first predetermined sequence;

sampling and respectively storing analog reset signals from a plurality of pixels of said sensor according to a second predetermined sequence;

subsequently combining and outputting all sampled and respectively stored analog output signals on a first line; and

combining and outputting all sampled and respectively stored analog reset signals on a second line.

11. (Previously Presented) The method according to claim 10, wherein said step of sampling said analog output signals comprises storing each analog output signal in a respective capacitive element of a first plurality of capacitive elements according to said first predetermined sequence.

12. (Previously Presented) The method according to claim 10, wherein said step of sampling said analog reset signals comprises storing each analog reset signal in a respective capacitive element of a second plurality of capacitive elements according to said second predetermined sequence.

13. (Previously Presented) The method according to claim 10, wherein said first and second predetermined sequences are determined by a less-than-full pixel resolution condition.

14. (Previously Presented) The method according to claim 13, wherein said first and second predetermined sequences further comprise interpolating different row output and reset signals from a column readout circuit in said active image sensor.

15. (Previously Presented) The method according to claim 14, wherein said predetermined sequence further comprises sampling identical colors from different rows from a column readout circuit in said active image sensor.

16. (Previously Presented) The method according to claim 13, wherein said first and second predetermined sequences further comprise interpolating different column readout circuits in said active image sensor.

17. (Previously Presented) The method according to claim 10, wherein said first and second predetermined sequence is determined by a Bayer pattern.

18. (Previously Presented) The method of claim 10, further comprising:

subtracting said combined analog output signal from said combined analog reset signal.

19. (Previously Presented) The method of claim 18 further comprising:

calculating a color separation value of said sampled signals of said sensor.

20. (Currently Amended) A charge-domain readout circuit comprising:

a plurality of column readout circuits each of which sample and combine multiple pixel signals and reset signal values of a plurality of pixels of an active pixel sensor, wherein each column readout circuit is associated with a respective column of sensors in said active pixel sensor, each of said plurality of column readout circuits comprising:

a plurality of charge storage devices for respectively storing each of said multiple pixel signals and reset signal values, and

a combining circuit for combining said respectively stored multiple pixel signals and reset signal values;

a first bus for receiving pixel signal values stored by a selected one of said column readout circuits; and

a second bus for receiving said reset signal values stored by a selected one of said column readout circuits.

21. (Canceled)

22. (Currently Amended) The circuit of claim [[21]] 20, wherein ~~each sample and hold circuit comprises~~:

~~a plurality of charge storage elements; and~~

each of said combining circuits comprises a plurality of first switches,

wherein said plurality of charge storage devices comprises a plurality of charge storage elements,

wherein each of said plurality of first switches ~~being~~ is coupled to a respective one of said plurality of charge storage elements, and

wherein said plurality of first switches can be selectively enabled to sample a signal from a sensor in said array to be stored by said charge storage element.

23. (Previously Presented) The circuit of claim 22, wherein each column readout circuit comprises a plurality of second switches which can be selectively enabled to hold one side of said charge storage elements at a reference voltage when a corresponding one of said first switches is enabled to sample a value from a sensor.

24. (Previously Presented) The circuit of claim 22, wherein each column readout circuit comprises a switch that can be selectively enabled to short together one side of each plurality of charge storage elements.

25. (Previously Presented) The circuit of claim 20, further comprising column switches coupled between each of said column readout circuits, wherein said column switches can be selectively enabled to couple together said stored pixel signal and reset signal values present on said column of sensors in said active pixel sensor.

26. (Currently Amended) A method of reading out values from active pixel sensors in an array of sensors, comprising:

selecting multiple rows of sensors whose values are to be read out;

storing correlated double sampled values for a plurality of sensors in said selected rows, wherein said values for each sensor are stored by a respective pair of charge storage devices in a readout circuit associated with a column in said array in which said sensor is located;

combining said stored signals; and

sensing said stored values associated with said plurality of sensors in said selected rows using an operational amplifier-based charge sensing circuit that is common to said readout circuits.

27. (Previously Presented) The method of claim 26 wherein said act of storing correlated double sampled values comprises sampling and storing a signal value of a sensor and sampling and storing a reset value of said sensor.

28. (Previously Presented) The method of claim 27 including setting a reference voltage on first sides of respective ones of a plurality of capacitive elements and subsequently coupling said signal and reset values to second sides of said respective ones of a plurality of capacitive elements.

29. (Previously Presented) The method of claim 28 wherein setting a reference voltage comprises providing said reference voltage to said common operational amplifier-based charge sensing circuit.

30. (Previously Presented) The method of claim 29 wherein sensing said stored values comprises using a crowbar switch to force charge stored in each respective readout circuit onto feedback capacitive elements in said operational amplifier-based charge sensing circuit.

31. (Currently Amended) A processing system, comprising:

a processing circuit;

an imaging circuit coupled to said processing circuit, said imaging circuit having a charge-domain readout circuit, said readout circuit comprising:

a plurality of column readout circuits each of which sample and combine multiple pixel signal and reset values of a plurality of pixels of an active pixel sensor, wherein each column readout circuit is associated with a respective column of sensors in an active pixel sensor, each of said plurality of column readout circuits comprising:

a plurality of charge storage devices for respectively storing each of said multiple pixel signals and reset signal values, and

a combining circuit for combining said respectively stored multiple pixel signals and reset signal values;

a first bus for receiving pixel signal values stored by a selected one of said column readout circuits; and

a second bus for receiving said pixel reset values stored by a selected one of said column readout circuits.

32. (Canceled)

33. (Currently Amended) The processing system of claim [[32]] 31, wherein ~~each sample and hold circuit comprises~~:

~~a plurality of charge storage elements; and~~

each of said combining circuits comprises a plurality of first switches,

said plurality of charge storage devices comprises a plurality of charge storage elements,

each of said plurality of first switches ~~being~~ is coupled to a respective one of said plurality of charge storage elements, and

wherein said plurality of first switches can be selectively enabled to sample a signal from a sensor in said array to be stored by said charge storage element.

34. (Previously Presented) The processing system of claim 33, wherein each column readout circuit further comprises a plurality of second switches which can be selectively enabled to hold one side of said charge storage elements at a reference voltage when a corresponding one of said first switches is enabled to sample a value from a sensor.

35. (Previously Presented) The processing system of claim 34, wherein each column readout circuit comprises a switch which selectively can be enabled to short together one side of each plurality of charge storage elements.

36. (Previously Presented) The processing system of claim 35, further comprising column switches coupled between each of said column readout circuits, wherein said column switches can be selectively enabled to couple together said stored pixel signal and reset values present on said column of sensors in said active pixel sensor.